MAHARAJA AGRASEN COLLEGE

University of Delhi

Vasundhara Enclave, Delhi 110096

Curriculum Vitae

First Name	Dr. VANDANA	Middle Name		Last Name	KUMARI
Designation	Assistant Professor		Department	Electronics	
Date of Birth	6th June 1986		Date of Joining	8th August 2014	
Residential Address	RZ- 35-36, V-Block, Vishu Vihar, Uttam Nagar, New Delhi-59				
Contact No.	9971657377		Email Id	vandanakumari@mac.du.ac.in	

Educational Qualifications

Degree	Institution	Year	Details
Ph. D	University of Delhi	2014	Microelectronics
M. Sc	University of Delhi	2009	Electronics
B. Sc	University of Delhi	2006	Electronics
Specialization	Semiconductor Devices – Modeling and Simulation		

Publication Index

Papers in referred International journal:	**38**
Papers in International conferences:	**26**
Papers in National conference:	**3**
Book Chapter:	**8**
H index:	**10**
Total Citation:	**227**

Career Profile

Organization/ Institution	Post Held	Adhoc/ Temp/ Permanent	From	To	Total Experience
Maharaja Agrasen College, University of Delhi	Assistant Professor	Adhoc	August 2014	Till date	8 years 4 months
Keshav Mahavidyalaya	Assistant Professor	Adhoc	Jan 2014	April 2014	4 months

MAHARAJA AGRASEN COLLEGE
University of Delhi
Vasundhara Enclave, Delhi 110096

List of research papers published in peer reviewed/ UGC Listed/ Scopus indexed research journals

Title of the article / paper	Journal Name	ISSN	Issue / Vol No.	Year	Whether Peer reviewed/ UGC Listed/ Scopus Indexed Journal	Thomson Reuter Impact Factor
Temperature Dependent Drain Current Model for Gate Stack Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET For Wide Operating Temperature Range	Microelectronics Reliability (MER),	0026-2714	52	2012	yes	1.418
Simulation Study of Insulated Shallow Extension Silicon On Nothing (ISESON) MOSFET for High Temperature applications	Microelectronics Reliability (MER),	0026-2714	52	2012	yes	1.418
Two Dimensional analytical Drain Current Model for Double Gate MOSFET Incorporating Dielectric Pocket (DP-DG)	IEEE Transactions On Electron Device (TED)	0018-9383	59	2012	yes	2.917
Digital Circuit Analysis of Insulated Shallow Extension Silicon On Void (ISESOV) FET for Low Voltage Applications	*SPIE Digital Library*		8549	2012	yes	--
Analog and digital Performance Assessment of Empty Space in Double Gate (ESDG) MOSFET: A	*Journal of Computational and Theoretical Nanoscience (JCTN)*	1546-1955	13	2013	yes	--

Novel Device Architecture						
Investigation of Empty Space in Nanoscale Double Gate (ESDG) MOSFET for High Speed Digital Circuit Applications	*Journal of Semiconductor Technology and Science (JSTS*	1598-1657	13	2013	yes	--
Circuit Level Implementation for Insulated Shallow Extension silicon On Nothing (ISE-SON) MOSFET: A Novel Device architecture	*IETE Journal of Research (JR),*	0377-2063	59	2013	yes	1.877
Performance Investigation of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET for Low Voltage Digital Applications	*Journal of Semiconductor Technology and Science*	1598-1657	13	2013	yes	--
Comparative Study of Silicon On Nothing and III-V On Nothing Architecture for High Speed and Low Power Analog and RF/Digital Applications	*IEEE Trans. On Nanotechnology*	1536-125X	12	2013	yes	2.967
Analytical Modeling of Dielectric Pocket Double Gate (DP-DG) MOSFET Incorporating Hot Carrier Induced Interface Charges	*IEEE Transactions on Device and Material Reliability*	1530-4388	14	2014	yes	1.886
Investigation of Electrostatic Integrity of Nanoscale Dual	IEEE Trans. On Nanotechnology	1536-125X,	13	2014	yes	2.967

Material Gate Dielectric Pocket Silicon On Void (DMGDPSOV) MOSFET for Improved Device Scalability						
Modeling and Simulation of Double Gate Junctionless Transistor Considering Fringing Field Effects	Solid State Electronics	0038-1101	107	2015	yes	1.916
Theoretical Investigation of Dual Material Junctionless Double Gate Transistor for Analog and Digital Performance	IEEE Trans. On Electron Devices	0018-9383	62	2015	yes	2.917
Nanoscale-RingFET: An Analytical Drain Current Model Including SCEs	IEEE Trans. On Electron Devices,	0018-9383	62	2015	yes	2.917
Modeling and Simulation of Nanoscale Lateral Gaussian Doped Channel Asymmetric Double Gate MOSFET	Journal of NanoResearch	1661-9897	62	2016	yes	-
Nanoscale T-shaped Double Gate DG MOSFET: Numerical Investigation for Analog/RF and Digital Performance	*Superlattices and Microstructures*	0749-6036	89	2016	yes	3.12
Underlapped FinFET on insulator: Quasi3D analytical model	Solid State Electronics	0038-1101	129	2017	yes	1.916
Analytical Drain Current Model for Gate and Channel Engineered RingFET (GCE-RingFET	*Superlattices and Microstructures*	0749-6036	111	2017	yes	3.12

Sub-threshold Drain Current model of Double Gate RingFET (DG-RingFET) Architecture: An Analog and Linearity Performance Investigation for RFIC Design	*IETE Technical Review* (TR	: 0974-5971	35	2018	yes	1.932
Empirical Model for Nonuniformly Doped Symmetric Double-Gate Junctionless Transistor	IEEE Trans. On Electron Devices	0018-9383	65	2018	yes	2.917
Reconnoiter the leavening of Skin Deep Insulated Extension on Analog Performance of RingFET (SDIE-RingFET	AEU-Internation Journal of Electronics and Communication	1434-8411	83	2018	yes	3.169
Study of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) Transistor Including Source Drain Depletion Length: Model for Sub-threshold Behaviour	*Superlattices and Microstructures*	0749-6036	113	2018	yes	3.12
Temperature Based Analysis of 3-Step Field Plate AlGaN/GaN HEMT using Numerical Simulation	Advances in Natural Sciences: Nanoscience and Nanotechnology	2043-6262	10	2019	yes	--
Assessment of Dual-Gate AlGaN/GaN MISHEMT for high temperature DC to DC converter	*Superlattices and Microstructures*	0749-6036	144	2020	yes	3.12
Gate Stacked Dual-Gate MISHEMT with 39THz·V Johnson's Figure of Merit for V-band applications	Journal of Computational Electronics	1572-8137	20	2020	yes	1.983
TCAD Based Optimization of Field Plate Length &	*IETE Technical Review* (TR	: 0974-5971	-	2020	yes	1.932

Passivation Layer of AlGaN/GaN HEMT for Higher Cut-off Frequency & Breakdown Voltage						
Optimization of π – Gate AlGaN/AlN/ GaN HEMTs for Low Noise and High Gain Applications	Silicon	1876-9918	14	2020	yes	2.67
Sensitivity Assessment of RingFET Architecture for the Detection of Gas Molecules: Numerical Investigation	*IETE Technical Review* (TR	: 0974-5971	38	2021	yes	1.932
TCAD Investigation of Total Ionizing Dose (TID) Effects on Gallium Nitride HEMTs	Silvaco's Simulation Standard		31	2021	yes	--
Impact of Heavy Ion Particle Strike Induced Single Event Transients on Conventional and π – Gate AlGaN/GaN HEMTs	Semiconductor Science and Technology	1361-6641	36	2021	yes	2.352
TCAD-Based Assessment of Dual-Gate MISHEMT with Sapphire, SiC, and Silicon Substrate	*IETE Technical Review* (TR	: 0974-5971	38	2021	yes	1.932
TCAD-Based Investigation of Double Gate JunctionLess Transistor for UV Photodetector	IEEE Trans. On Electron Devices	0018-9383	68	2021	yes	2.917
Impact of Non-Uniform Doping on the Reliability of Double Gate JunctionLess Transistor: A Numerical Investigation	*IETE Technical Review* (TR	: 0974-5971		2021	yes	1.932
TCAD based Investigation of Single Event Transient Effect in Double Channel AlGaN/GaN HEMT	IEEE Transactions on Device and Materials Reliability	1530-4388	21	2021	yes	1.886

TCAD investigation for Dual-Gate MISHEMT with Improved Linearity and Current Collapse for LNAs	*IETE Technical Review* (TR	: 0974-5971		2021	yes	1.932
E-mode All-GaN-Integrated Cascode MISHEMT with GaN/InAlGaN/GaN backbarrier for high power switching performance: Simulation Study	*Superlattices and Microstructures*	0749-6036		2021	yes	3.12
Investigation of proton irradiated dual field plate AlGaN/GaN HEMTs: TCAD based assessment	Microelectronics Journal	0026-2692	122	2022		1.992
Interplay between γ – ray Irradiation and 3DEG for Dosimeter Applications	IEEE *Access*	*2169-3536*	10	2022		3.367

List of Books (edited/ authored)

Title of the book	Author / Editor	ISBN	Year	Publisher

List of Chapters in a book

Title of the chapter	Title of the book	ISBN	Year	Publisher
Variability Investigation of Double Gate JunctionLess (DG-JL) Transistor for Circuit Design Perspective	VLSI Design and Test	978-981-10-7470-7	2017	Springer Singapore
Study of Extended Back Gate Double Gate JunctionLess Transistor: Theoretical and Numerical Investigation	The Physics of Semiconductor Devices	978-3-319-97604-4	2017	Springer, Cham

Optically Controlled Silicon On Nothing MOSFET-Numerical Simulation	The Physics of Semiconductor Devices	978-3-319-97604-4	2017	Springer, Cham
Threshold Voltage Investigation of Recessed Dual-Gate MISHEMT: Simulation Study	VLSI Design and Test. VDAT 2018, Communications in Computer and Information Science	ISBN978-981-13-5950-7	2019	Springer Singapore
An Asymmetric π – Gate MOSHEMT Architecture for High Frequency Applications	Lecture Notes in Networks and Systems,	ISBN978-981-15-8366-7	2019	Springer
Gate Leakage Current Assessment of AlGaN/GaN HEMT with AlN Cap Layer	Lecture Notes in Networks and Systems,	ISBN978-981-15-8366-7	2019	Springer
Comparative Study of AlGaN/GaN HEMT and MOS-HEMT Under Positive Gate Bias Induced Stress	Lecture Notes in Networks and Systems,	ISBN978-981-15-8366-7	2019	Springer
Numerical Investigation of Gate Field Plate AlGaN/GaN HEMT with Multi- Recessed Buffer	Lecture Notes in Networks and Systems,	ISBN978-981-15-8366-7	2019	Springer

List of Papers presented/ Invited Lecture/ Resource Person in conferences/ seminars/ workshops/ FDPs

Title of Paper/ Talk/ Subject	Conference/ Invited talk/ Resource Person	Title of conference/ seminar/ workshop/ FDP	Level (College/ State/ National/ International)	Year	Name of Organizer(s)
Simulation Study of Gate Stacked Insulated Shallow Extension Silicon On Nothing ISE-	Conference	IEEE Student's Technology Symposium		2011	IEEE

SON MOSFET for RFICs design				
Comparative Study of Dielectric Pocket (DP) MOSFET Incorporating Buried Oxide Layer (BOX) with DP MOSFET for RF Applications	Conference	International symposium on Microwave and Optical Technology (ISMOT-2011),	2011	
Analog Performance of Insulated Shallow Extension Silicon On Nothing (ISE-SON) MOSFET: Simulation study	Conference	VLSI Design and Test symposium (VDAT-2011),	2011	VLSI society of India
Laterally Asymmetric Channel Insulated Shallow Extension Silicon On Nothing LAC-ISE-SON MOSFET for Improved Reliability and Digital Circuit simulations	Conference	International Conference on Circuit Devices and Systems (ICDCS-2012),	2012	IEEE
Theoretical Investigation of Back Gate Bias on the Electrostatic Integrity of Insulated shallow Extension silicon On void (ISESOV) MOSFET	Conference	Innovation in Social and Humanitarian Engineering (INDICON 2012),	2012	IEEE
Temperature Dependent Model for Dielectric Pocket Double Gate (DPDG) MOSFET: A Novel Device Architecture	Conference	International Conference on Emerging Electronics (ICEE 2012),	2012	IEEE
Charge Based Modeling of channel Material Engineered P-type Double Gate MOSFET	Conference	International Conference on Emerging Electronics (ICEE 2014),	2014	IEEE

Sub-threshold Drain Current Model of Shell-Core Architecture Double Gate JunctionLess Transistor	Conference	IEEE Electron Device Kolkata Conference (2018 EDKCON)	2018	IEEE
RingFET Architecture for High Frequency Applications: TCAD Based Assessment	Conference	IEEE Electron Device Kolkata Conference (2018 EDKCON)	2018	IEEE
Reliability Comparison of Conventional & Two Finger AlGaN/GaN HEMT	Conference	IMRAC-2019	2019	IEEE
Three days National workshop on "Challenges of Teaching Physics Laboratory Courses in Online Mode	Conference	National workshop	2021	NASI

Mentored students under Science Academies' Summer Research Fellowship Programme, Joint Science Academies Panel, Indian Academy of Sciences (IASc), Bangalore, India

S. No.	Name	Year
1.	Neha Bhushan	2011
2.	Neel Modi	2013
3.	Aravindin Ilango	2014
4.	K. Shermetha	2015
5.	Ayush Kumar	2016
6.	Abhineet Sharan	2017
7.	Khushwant Sehra	2018
8.	Shreyasi Das	2019
9.	Amrutamayee Nayak	2019
10	Shreyasi Das	2020

Other Responsibilities

- **Joint Secretary**- IEEE EDS Delhi Chapter 2019-till date
- **Treasurer**- IEEE EDS Delhi Chapter 2015-2018
- Member of Institute of Electrical and Electronic Engineering ***IEEE*** (2010-2014--**Student Member,** 2015-till date---**Member**) (90853888)

MAHARAJA AGRASEN COLLEGE
University of Delhi
Vasundhara Enclave, Delhi 110096

- **Member** of ***IEEE*** Electron Device Society ***IEEE-EDS*** (2010-2014--**Student Member,** 2015-till date---**Member**) (90853888)
- **Member of IEEE WIE- 2017- till date** (90853888)
- **Treasurer**-2nd National Conference On Recent Development in Electronics (**NCRDE-2017**)
- **Member Local Organising Committee**- 1st National Conference On Recent Development in Electronics (**NCRDE-2013**)
- **Co-Convener-** IEEE EDS DL talk by Prof. Merlyne De Souza on "CMOS Scaling: Negative Capacitance and Challenges Ahead" on 03rd December 2021.
- **Co-Convener-** Technical talk by Ms. Rekha Jain on "5G- Be ready for the future" on 04th December 2021.
- **Coordinator**- TWO DAYS ONLINE LECTURE SERIES on "Fundamentals and Applications of Technology Driven Sensors" during 24th - 25th september 2021.

I certify that the information given above is correct and factual to the best of my knowledge.

Date: