Intelligent Energy Information and Management System for Academic Institutes

Advances in Solar Power Generation and Energy Harvesting pp 99-108 | Cite as

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Conference paper
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Abstract

Requirement of energy for human sustenance and growth has increased exponentially during the last century. The rate of rise in demand for energy has reached unprecedented levels leading to widening of gap between demand and supply of electric energy due to the scarcity of resources. The harmful effects of excessive usage of energy on the environment pose a great danger to the sustainability of our ecosystem. In this scenario, it becomes pertinent to design a strategy for increased efficiency of electricity utilization with an aim to minimize air pollution and carbon footprint. Hence, energy management systems are the need of the hour to identify the potential for improvements in energy efficiency. However, the implementation of Energy Information and Management System (EIMS) in academic institutes is extremely limited due to lack of awareness and relevant green policies. The current work presents a blueprint of Energy Information and Management System for an academic institute leading to multi-measure energy efficiency through multiple strategies including equipment operational improvements and upgrades, and occupant behavioural changes. The design of Intelligent EIMS enables energy savings relative to a baseline model, which predicts energy consumption from key parameters such as occupancy levels mapped with the timetable and operational schedule. The need for policies to be adopted by educational institutes for optimum utilization of electrical energy has been discussed and presented in the paper. In the present work, the different sub-domains/facilities of the college were primarily divided into three categories, namely facilities mapped with college timetable (like classrooms, laboratories, etc.), facilities mapped with fixed or regular schedule (like hostel mess, corridors, etc.) and facilities independent of college timetable or fixed schedule (like

canteen, staffroom, common room, etc.). The two basic categories were further subdivided on the basis of scheduled usage and ad hoc usage of these facilities. Based on these categorizations, policies for energy usage were framed for these facilities, and prototype EIMS was designed and implemented at Maharaja Agrasen College, University of Delhi. 4.8% saving in the power consumption was observed post-EIMS implementation.

Keywords

Energy information system Energy management RS-485 network Baselining Benchmarking Green policy for academic institutes Energy efficiency EIMS in academic institutes

Notes

Acknowledgements

Design of energy information system (EIS) has been financed by University of Delhi, Innovation Project MAC101: "Measuring Environmental Footprint of University of Delhi and Transforming it into a Zero-Impact University". The authors would like to thank the Principal Investigators Dr. A. Pundir, Dr. V. Pundir and Dr. P. Rai for their contribution during the course of work.

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Personalised recommendations

Compact Mode Division (de)Multiplexer Based on Collaterally Coupled SOI Waveguides

Publisher: IEEE Cite This PDF

Jyoti Prasad Nath ; Nikhil Dhingra ; Geetika Jain Saxena ; Enakshi K. Sharma **All Authors**

Abstract: We present the design of a compact 5-mode division (de)multiplexer based on silicon-on-insulator waveguides for on-chip optical interconnects. The configuration consists ... **View more**

Metadata

Abstract:
We present the design of a compact 5-mode division (de)multiplexer based on silicon-on-insulator waveguides for on-chip optical interconnects. The configuration consists of two coupled sections where each section comprises of two collocated asymmetric directional couplers to couple light from two input waveguides carrying independent signals into two TE modes (TE_1, TE_2 or TE_3, TE_4) of an interconnect trunk waveguide. For coupling into the TE_0 mode of the trunk waveguide, an adiabatic taper is used to connect a fifth input waveguide. The proposed design with collocated directional couplers offers an advantage of a small footprint compared to sequential designs. The total coupling length of the device for multiplexing TE_1 to TE_4 modes is only 38.89 µm. In addition, the device exhibits low insertion loss ~0.24 dB and crosstalk better than -33 dB at the design wavelength of 1550 nm.

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INSPEC Accession Number: 19565779

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Design of a Compact Low-Loss Phase Shifter Based on Optical Phase Change Material

Publisher: IEEE

Nikhil Dhingra ; Junchao Song ; Geetika J. Saxena ; Enakshi K. Sharma ; B. M. A. Rah… **All Authors**

Abstract: We propose the design of a nonvolatile, low-loss optical phase shifter based on optical phase change material (O-PCM). The optical phase change material Ge 2 Sb 2 Se 4 Te... **View more**

Metadata

Abstract:
We propose the design of a nonvolatile, low-loss optical phase shifter based on optical phase change material (O-PCM). The optical phase change material $Ge_2Sb_2Se_4Te_1$ (GSST), which exhibits low loss at telecommunication wavelength 1.55 μm as compared to other commonly used O-PCMs, is used in this work as the active material. Instead of direct interaction of the waveguide mode with the O-PCM, the design utilizes coupling between the primary SiN strip waveguide and a waveguide formed by O-PCM, in its amorphous state. The phase matching in the amorphous state inhibits the interaction of the waveguide mode with GSST in its highly lossy crystalline state resulting in low loss operation. Due to a high differential refractive index between the two states of GSST, the design requires a very small length of the phase shifter to accumulate the desired phase difference. The overall response of the Mach-Zehnder Interferometer (MZI) configuration using the designed phase shifter shows that the design can be used to obtain optical switching with a very small insertion loss and crosstalk over the entire C-band.

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INSPEC Accession Number: 19184816

Design, Simulation and Comparative Analysis of Different Types of Solar Charge Controllers for Optimized Efficiency

Publisher: IEEE

Ashita Victor ; Dharmendra Kumar Mahato ; Amit Pundir ; Geetika Jain Saxena **All Authors**

Abstract

Abstract: The solar charge controller is designed to interface a PV (Photovoltaic) panel with a Lead-Acid battery for efficient charging of the battery. It is crucial to select the... **View more**

Metadata

Abstract:
The solar charge controller is designed to interface a PV (Photovoltaic) panel with a Lead-Acid battery for efficient charging of the battery. It is crucial to select the right charge controller. It is designed considering the non-linear characteristics of the PV panel and the charging and discharging profile of the battery. The charge controllers are designed on MATLAB/Simulink and then implemented with hardware. There are three types of charge controllers: the basic charge controller using voltage regulator, Pulse Width Modulation (PWM) based and the Maximum Power Point Tracking (MPPT) based charge controllers. Each charge controller works best for a set of parameters. Thus, parameters such as panel's voltage/current rating, cost,operating temperature etc. are taken into consideration for choosing the right charge controller. The basic charge controller results in inefficient charging of the battery, thus, the PWM based and the MPPT based charge controllers are designed.

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Assessment of Dual-Gate AlGaN/GaN MISHEMT for high temperature DC to DC converter

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Modeling
Dual-gate
Converter

ABSTRACT

Numerical assessment of Dual-Gate AlGaN/GaN MISHEMT have been presented in this paper. Analytical model has been developed and the various parameters extracted are surface potential, electric field and threshold voltage for different device specifications. Threshold voltage of nearly 0.15 V has been computed which is nearly same to that of simulated Dual-Gate MISHEMT. Simulations have been performed using ATLAS TCAD tool. Dual-Gate MISHEMT with different gate dielectric materials such as Si_3N_4 and gate stack combinations like HfO_2/Al_2O_3 has been analyzed. From the results it has been inferred that at higher temperature, drain current and transconductance reduces due to lower electron sheet concentration. Different combinations of gate biases (applied at the second gate i.e. Gate 2 presented near the drain side) has been used for optimizing the device parameter for better switching performance. For DG-MISHEMT with barrier thickness of 22 nm (both the gates connected together), I_{ON}/I_{OFF} ratio reduces from 10^9 to 10^6 for high temperature (upto 423 K) due to reduced sheet carrier concentration. For inductance load, output drain voltage exhibits voltage range of 9.2V/2.3V for gate pulse of -8V/+2V with 30% duty cycle. Also, it is seen that as barrier thickness is varied from 18 nm to 30 nm, I_{OFF} increases and results in reduced output drain voltages. Performance of Single Gate and Double Gate MIS-HEMTs has also been compared for DC-to DC converter using inductance load circuit.

1. INTRODUCTION

With the growing demand for energy consumption (i.e. expected to increase by nearly 40% worldwide in next 20 years), highly efficient power devices are needed for power electronics [1]. Devices based on wide bandgap materials such as GaN and SiC, have become alternative to dominant silicon-based devices and meet the continuous demand of high voltage, current and power handling capability [2]. Due to properties such as wide bandgap, high saturation velocity and high breakdown voltage, GaN High-Electron-Mobility-Transistors (HEMTs) have demonstrated their candidature for future high frequency [3–5] and high-power applications [6–10]. High sheet carrier densities with carrier mobilities upto 2000 $cm^2V^{-1}.s^{-1}$ have been achieved in such devices and this results in increased power densities and current drive capability as compared to devices based on Si or GaAs counterparts [11, 12]. Countless applications of GaN HEMTs have been reported recently such as power switch [13], dc-to-dc converter [14], resonant converters [15], motor drives [16] etc. GaN power switch for kW power conversion with switching speed more than 2 MHz, reduced

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Gate stacked dual-gate MISHEMT with 39 THz·V Johnson's figure of merit for V-band applications

Preeti Singh[1] · Vandana Kumari[2] · Manoj Saxena[3] · Mridula Gupta[1]

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Abstract
In this investigation, extensive simulations were performed for an AlGaN/GaN Dual-Gate MISHEMT configuration using ATLAS TCAD to optimize the device design for high power switching applications. We conducted a simulation study for the breakdown characteristics of a Dual-Gate AlGaN/GaN (DG)-MISHEMT with different gate lengths as explained in this paper. The optimized device with 0.25 µm gate length exhibits an breakdown voltage > 700 V and an cut-off frequency of 50 GHz when gate2 (G2) is attached to the source and bias is applied at gate1 (G1). We studied the impact on a breakdown characteristics and the frequency performance of different dimensions such as distance between the two gates (L_{GG}), gate1-to-source distance (L_{G1S}) and gate1-to-drain distance (L_{G1D}). The optimized device design was further used to study the scattering-parameters for different gate combinations. Further improvement in breakdown voltage and Johnson's figure of merit ($f_T \times V_{BR}$) is achieved for the DG-MISHEMT with HfO_2–Al_2O_3 as gate insulator.

Keywords TCAD · Dual-Gate MISHEMT · Gate stack · S-parameter · Kink effect

1 Introduction

GaN based HEMTs have become the choice for high power and high frequency applications due to various advantageous physical parameters such as low on-resistance, high mobility, high thermal conductivity and high critical electric field [1–5]. Despite various outstanding physical and electrical properties, the reliability of AlGaN/GaN HEMTs is limited by the OFF-state breakdown voltage (V_{BR}) [6] and the kink effect in the scattering parameter (S_{22}) depending on biasing conditions [7]. Various techniques have been employed to improve the V_{BR} of these devices such as a field plate [8], a charged passivation layer [9], Fe or carbon buffer doping [10], optimizing buffer thickness [11] and introduction of a GaN cap layer [12]. GaN-HEMTs with single gate oxide or gate stacks exhibit lower gate leakage current than conventional AlGaN/GaN HEMTs [13], and hence improve breakdown characteristics. Numerous field plate techniques have been reported to improve the breakdown voltage of GaN based devices, namely gate-connected field plate structures [14], integrated slant field plates [15], floating or non-floating multiple-grated FP structures [16, 17] and FP structures with a high-K passivation layer [18]. These techniques manipulate the electric field intensity in the gate-drain access region and thus improve reliability of the device. Another technique that has been reported to reduce feedback capacitance is a dual-gate configuration [19], where the additional gate connected to the source terminal results in decreased Miller capacitance. In contrast, for gate [20] or source-connected FP techniques [21], the extension of a gate or source terminal, respectively, over the passivation layer, introduces additional parasitic capacitance between the gate-drain and drain-source terminals; this influences the frequency performance, power-added-efficiency performance [22] and the switching characteristics of the device [23]. Furthermore, it has been observed that the dual-gate configuration of AlGaN/GaN HEMT provides higher power gain as compared to a single-gate HEMT due to reduced feedback capacitance and higher output impedance [19]. Improvements in large signal characteristics and reliability tests under RF stress of AlGaN/GaN DG-HEMTs on

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ORIGINAL PAPER

Optimization of π – Gate AlGaN/AlN/GaN HEMTs for Low Noise and High Gain Applications

Khushwant Sehra[1] · Vandana Kumari[2] · Mridula Gupta[1] · Meena Mishra[3] · D. S. Rawal[3] · Manoj Saxena[4]

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Abstract
This paper presents a comprehensive TCAD based assessment to evaluate the intrinsic gain and minimum noise figure metrics of the T – Gate, and the π – Gate AlGaN/AlN/GaN HEMTs along with their recessed architectures. The work presented in this paper, to the best of author's knowledge, is first in its attempt to systematically bring out both the effect of minimum noise figure metrics and intrinsic gain at the device level for the π – Gate architecture and their recessed counterparts whilst evaluating its stability for high frequency operations. Comparison demonstrates an enhancement in intrinsic gain by 64.5% in case of asymmetric π – Gate and 77% for asymmetric recessed π – Gate in comparison to their T – Gate counterparts. Further, the said architectures possess a wider range of flat gain operation with suppressed values of minimum noise figure metrics. These modifications result in a modest trade off in the minimum noise figures when best case is considered and compared with their T – Gate counterparts. Additionally, it is also demonstrated that such device architectures demonstrate much stable high frequency operation in comparison to their primer. The results so presented establish the superiority of the π – Gate AlGaN/AlN/GaN HEMTs for low noise and high gain applications.

Keywords High Electron mobility transistors · Intrinsic gain · Minimum noise figure · Stern stability factor · Gate recess

1 Introduction

High Electron Mobility Transistors (HEMTs) have emerged as a promising candidate for high power and high frequency applications pertaining to wireless communications and satellite links. Among various III-V compound semiconductor, GaN based HEMTs possess high sheet carrier density and high electron mobility in the 2–D Electron Gas (2DEG) channel which accounts for high frequency operation [1–3]. GaN based devices were also capable to operate at high voltage and enables high frequency operation (>100GHz) [4–6]. The compatibility of wide bandgap semiconductors with power amplifiers not only results in enhancement of output power, but also increases the temperature tolerance and radiation hardness of the resulting circuits [7].

In past few years, various device configurations, such as field plate [8–13] and floating gate [14] have been studied for improvement of device breakdown voltage. Studies related to different passivation layers [15], substrates and gate insulation has also been reported to investigate their impact on various performance metrics of the device. Enhancement of carrier confinement with help of BGaN (Boron content ranging from 0.5% – 2%) as back – barrier has been proposed theoretically by Han et al. [16]. A novel E – mode HEMT device architecture possessing three – Dimensional Electron and Hole Gases (3DEG and 3DHG) was demonstrated by Deng et al. [17] with the combination of positive graded AlGaN barrier layer (GAL) and negative graded AlGaN back barrier layer (GABL). High – voltage induced stress leading to irreversible electrical degradation in HEMTs by courtesy of inverse piezoelectric effect and crack formation (more appropriately Nanocracks) in AlGaN epitaxial layer was experimentally and theoretically studied by Mazumdar et al. [18]. Apart from these, numerical models have been developed over the years

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TCAD-Based Optimization of Field Plate Length & Passivation Layer of AlGaN/GaN HEMT for Higher Cut-Off Frequency & Breakdown Voltage

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ABSTRACT

ATLAS TCAD-based comparative investigation (mainly breakdown voltage, cut-off frequency and leakage current) has been presented in this work for different length of gate field plate and source field plate. 127 V of breakdown voltage has been achieved at 0.25 μm gate length having 0.8 μm gate field plate length and 1 μm source field plate length. By amalgamating source field plate, maximum cut-off

frequency of 38 GHz was achieved at 0.25 μm channel length. Passivation layer permittivity and barrier thickness has also been used to optimize the device